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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,727	10/31/2003	Matthew L. Scidl	SUN-P9719-SPL	1586
57960	7590	06/30/2006	EXAMINER	
SUN MICROSYSTEMS INC.				MOORE, PATRICK M
C/O PARK, VAUGHAN & FLEMING LLP				ART UNIT
2820 FIFTH STREET				PAPER NUMBER
DAVIS, CA 95618-7759				2188

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/698,727	SEIDI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Patrick M. Moore	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 16 March 2006.

2a) This action is **FINAL**.                                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-4,6-14 and 16-21 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-4,6-14 and 16-21 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. Claims 1, 6, 10, 11, 16, 20 & 21 have been amended.
2. Claims 5 & 15 have been cancelled.
3. Claims 1-4, 6-14 & 16-21 remain pending in the application.

#### ***Specification***

4. Acknowledgement is made of the amendments to the specification as received on **16 March 2006**.

#### ***Response to Amendment***

5. Applicant's amendments and arguments filed on **16 March 2006**, in response to the Office Action mailed on **12 January 2006**, have been fully considered, but are not persuasive. Therefore, the rejections made in the previous Office Action are maintained and restated below, with changes as needed to address the amendments.

#### ***Claim Rejections - 35 USC § 102***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-21 are rejected under **35 U.S.C. 102(b)** as being anticipated by Chopra et al. (US Patent # 6,412,043), herein referred to as Chopra.
  - a. **As per Claim 1**, Chopra discloses a method for supporting read-only objects within an object-addressed memory hierarchy, comprising: receiving a request at a translator to access an object, wherein the request includes an object identifier for the object that is used to reference the object within the object-addressed memory hierarchy [**Figure 9, # 200, # 212 & Column 41, Lines 3-10**], wherein

the translator translates between object identifiers (used to reference objects in an object cache) and physical addresses (used to address objects in main memory) **[a “TLB” as defined in Column 1, Lines 22-24]**; using the object identifier to retrieve an object table entry associated with the object **[Figure 9, # 212 & Column 41, Lines 23-24]**; if the request is a write request **[Column 41, Lines 3-4]**, examining a read-only indicator within the object table entry **[Figure 9, # 212, 214 & Column 41, Lines 25-29]**, if the read-only indicator specifies that the object is a read-only object, performing a corrective action to deal with the fact that the write request is directed to a read-only object **[Figure 9, # 218 & Column 41, Lines 31-35]**.

- b. **As per Claim 2**, Chopra further discloses the method of claim 1, wherein if the request is a read request, the method further comprises using a physical address from the object table entry to access the object in main memory **[Figure 9, # 222, Figure 10, #248, Column 41, Lines 53-59 & Column 42, Lines 34-40]**.
- c. **As per Claim 3**, Chopra further discloses the method of claim 1, wherein performing the corrective action can involve causing a fault handler in the requesting processor to perform the corrective action **[Figure 9, # 218 & Column 41, Lines 31-35]**.
- d. **As per Claim 4**, Chopra further discloses the method of claim 1, wherein performing the corrective action can involve: obtaining a writable copy of the object, clearing the read-only indicator to indicate that the object is no longer read-only, and updating the writable copy of the object with data from the write

request [Column 17, Lines 4-20]; updating a remotely located master copy of the object with data from the write request [Column 27, Lines 48-55]; terminating the requesting process because the write request is not allowed [Column 43, Lines 41-55]; and if the request is directed to a debugging breakpoint, pausing the requesting process and clearing the read-only indicator [Column 14, Lines 42-59].

- e. **As per Claim 6**, Chopra further discloses the method of claim 1, wherein prior to receiving the request at the translator, the request is initially directed to the object cache [Figure 9, #202, 204 & Column 41, Lines 4-8]; wherein if the request causes a hit in the object cache, the object is accessed in the object cache and the request is not sent to the translator [“Yes” branch of Figure 9, # 204 & Column 41, Lines 9-15]; and wherein if the request causes a miss in the object cache, the request is sent to the translator [“No” branch of Figure 9, # 204 & Column 41, Lines 9-10].
- f. **As per Claim 7**, Chopra further discloses the method of claim 6, further comprising making a given object read-only by: setting a read-only indicator associated with the given object to indicate that the given object is read-only [“first instruction” in Column 46, Line 56]; causing all object caches within a local cache-coherent domain to flush any modified cache lines of the given object out to main memory [“first operation” in Column 46, Line 48]; whereby subsequent upgrades of the given object from read-only status to writable or

modified status in any caches within the local cache-coherent domain must go through a translator [Column 47, Lines 8-14].

- g. **As per Claim 8**, Chopra further discloses the method of claim 7, wherein causing all object caches within the local cache-coherent domain to flush any modified cache lines of the given object out to main memory involves executing a read-with-intent-to-only-read (RWITOR) instruction on each cache line of the given object [Column 19, Lines 35-47]. *Chopra defines a “SYNCO” instruction to function as a special flush mechanism, which dumps cache objects to main memory.*
- h. **As per Claim 9**, Chopra further discloses the method of claim 7, wherein the given object can be made read-only in response to a request received from outside the local cache-coherent domain [Column 44, Lines 17-40].
- i. **As per Claim 10**, Chopra further discloses the method of claim 1, wherein the translator includes hardware to translate between object identifiers and physical addresses [Figure 1, # 110].
- j. **As per Claim 11**, Chopra discloses an apparatus that supports read-only objects within an object-addressed memory hierarchy, comprising: a receiving mechanism configured to receive a request at a translator to access an object, wherein the request includes an object identifier for the object that is used to reference the object within the object-addressed memory hierarchy [Figure 9, # 200, # 212 & Column 41, Lines 3-10], wherein the translator translates between object identifiers (used to reference objects in an object cache) and physical

addresses (used to address objects in main memory) [a “TLB” as defined in **Column 1, Lines 22-24**]; a translation mechanism configured to use the object identifier to retrieve an object table entry associated with the object [**Figure 9, # 212 & Column 41, Lines 23-24**]; and a corrective action mechanism, wherein if the request is a write request [**Figure 1, # 218 & Column 41, Lines 31-35**], the corrective action mechanism is configured to, examine a read-only indicator within the object table entry [**Figure 9, # 212, 214 & Column 41, Lines 25-29**], and if the read-only indicator specifies that the object is a read-only object, to perform a corrective action to deal with the fact that the write request is directed to a read-only object [**Figure 1, # 218 & Column 41, Lines 31-35**].

- k. **Claim 12** is rejected under the same grounds as Claim 2.
- l. **Claim 13** is rejected under the same grounds as Claim 3.
- m. **Claim 14** is rejected under the same grounds as Claim 4.
- n. **Claim 16** is rejected under the same grounds as Claim 6.
- o. **Claim 17** is rejected under the same grounds as Claim 7.
- p. **Claim 18** is rejected under the same grounds as Claim 8.
- q. **Claim 19** is rejected under the same grounds as Claim 9.
- r. **Claim 20** is rejected under the same grounds as Claim 10.
- s. **As per Claim 21**, Chopra discloses a computer system that supports read-only objects within an object-addressed memory hierarchy, comprising: a processor [**Figure 1, # 100**]; the object-addressed memory hierarchy [**Figure 1, # 102**]; an object cache within the object-addressed memory hierarchy [**Figure 1, # 111**]; a

translator that translates between object identifiers, used to address objects in the object cache, and physical addresses, used to address objects in main memory [**Figure 1, # 110**]; a receiving mechanism within the translator configured to receive at the translator a request to access an object, wherein the request includes an object identifier for the object that is used to reference the object within the object-addressed memory hierarchy [**Figure 9, # 200, # 212 & Column 41, Lines 3-10**], wherein the translator translates between object identifiers (used to reference objects in an object cache) and physical addresses (used to address objects in main memory) [**a “TLB” as defined in Column 1, Lines 22-24**]; a translation mechanism within the translator configured to use the object identifier to retrieve an object table entry associated with the object [**Figure 9, # 212 & Column 41, Lines 23-24**]; and a corrective action mechanism, wherein if the request is a write request [**Figure 1, # 218 & Column 41, Lines 31-35**], the corrective action mechanism is configured to examine a read-only indicator within the object table entry [**Figure 9, # 212, 214 & Column 41, Lines 25-29**], and if the read-only indicator specifies that the object is a read-only object, to perform a corrective action to deal with the fact that the write request is directed to a read-only object [**Figure 9, # 218 & Column 41, Lines 31-35**].

***Response to Arguments***

7. Applicant's arguments filed **16 March 2006** have been fully considered but they are not persuasive. The following is an explanation as to non-persuasiveness for each of Applicant's arguments.

- a. As per Chopra's support of read-only objects, Examiner understands that Chopra expressly anticipates read-only objects within an object-address memory hierarchy in **Figure 9, #212, #214 & #218**. Furthermore, Examiner points out the following passages: "... the permission of the selected page is checked at step **#214...**" and "... then the page may be designated as *read only* initially, then the exception handler can update...", as disclosed by Chopra in **Column 41, Lines 25-29 & Column 41, Lines 41-42**, respectively. Therefore, Examiner understands Chopra to expressly disclose setting/examining a read-only indicator, as claimed by Applicant.
- b. As per Chopra's suggestion of a translator for translating an object address into a physical address, Examiner understands that Chopra expressly anticipates one such translator embodied as a TLB in **Column 1, Lines 22-24**. Examiner points out the passage: "... TLB or other resources to translate between logical and physical addresses", as disclosed by Chopra in **Column 1, Lines 23-24**. Furthermore, Examiner understands Applicant's amendment to Claims 1, 11 & 21 are meant to overcome the Prior Art rejection pertaining to Chopra. However, in addition to the above described anticipation, Examiner points out that Applicant has disclosed translation between "object identifiers and a physical

address" exists in the Prior Art as per Applicant's specification (see **Page 2, ¶0002, Lines 1-7** of the instant application). In summary, Examiner understands that Applicant's background section has admitted the claimed functionality exists in Prior Art.

c. As per Chopra's bypass of the TLB, Examiner understands that Chopra expressly anticipates a bypass of the TLB in the "**Yes**" branch of **Figure 9, # 204 & Column 41, Lines 9-15**. Specifically, Chopra discusses that "... if the determination at step **#204** was a vtag hit, then at steps **#206** and **#208** a check is made of the permissions..." in **Column 41, Lines 10-12**. Therefore, Examiner understands these steps embody a skipped access of the TLB, which is the result of following the "**No**" branch of **Figure 9, # 204** & described in **Column 41, Lines 9-10**.

#### ***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick M. Moore whose telephone number is (571) 272-1239. The examiner can normally be reached on M-F 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabahn can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



6/28/06

PMM

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